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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/729,734	12/05/2003	Wendy Lee Wilkins	783403605009	1308

7590 03/08/2006

Paul E. Franz
Jones Day
North Point
901 Lakeside Avenue
Cleveland, OH 44114

EXAMINER	
ANDUJAR, LEONARDO	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 03/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/729,734	WILKINS ET AL.
	Examiner	Art Unit
	Leonardo Andújar	2826

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13, 15, 16 and 25-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *14 and 17-24* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/03 & 07/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of species 2 (fig. 6, claims 1-13, 15, 16 and 25-32) in a communication filed on 03/01/2004 is acknowledged. The traversal is on the ground(s) that the claim 1 is generic. This is not found persuasive because in the restriction requirement set forth in the Office Action sent on 12/08/2005, it was clearly established that the application contains claims directed to patentably distinct species wherein each species is associated to each of the different embodiments depicted in the drawings. The examination of all the species is considered a serious burden since each species contains features that make them distinct and non-obvious over the other. Therefore, a complete and independent examination would be required for each of the disclosed species. Furthermore, the criterion for restriction of species is not whether the groups are coextensive but that the claims recite mutually exclusive characteristics of such species (MPEP § 806.04(f)). To traverse on the grounds that the species are not patentably distinct, the applicant should submit evidence, or identify such evidence in the record, showing the species to be obvious variants, or clearly admit on the record that this is the case. In either case, if the examiner finds one of the inventions unpatentable over the prior art, the evidence or admission may be used in a rejection under 35 U.S.C. 103(a) against the other invention(s). Because the applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 11, 13, 15, 16 and 25-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Ahn (US 6,392,269).

4. Regarding claim 1, Ahn (e.g. fig. 1) shows an integrated circuit apparatus 100 for facilitating the interconnection of one or more circuitry manufacture, comprising: a carrier substrate 110 defining a top surface and a bottom surface, the carrier substrate configured to receive one or more circuitry manufacture (bumps, traces) on the top surface and the bottom surface; one or more carrier substrate vias 18 penetrating the carrier substrate so that the carrier substrate vias define vias from the top surface to the bottom surface of the carrier substrate and further define interior via surfaces (e.g. fig. 3b), the one or more carrier substrate vias configured to receive one or more circuitry manufacture on the interior via surfaces (e.g. 38; fig. 3e); and one or more carrier substrate cavities, the one or more carrier substrate cavities formed on the top and/or bottom surfaces of the carrier substrate, the one or more carrier substrate cavities defining interior cavity surfaces and configured to receive one or more circuitry manufacture (140. 145, 171) on the interior cavity surfaces.

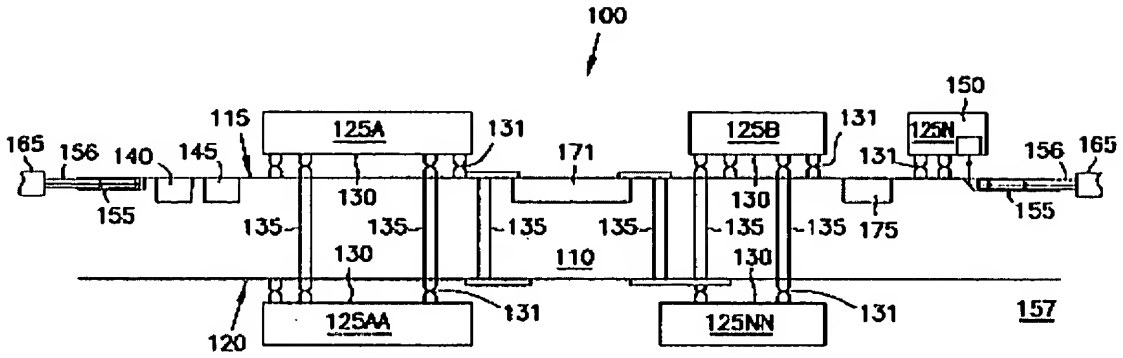
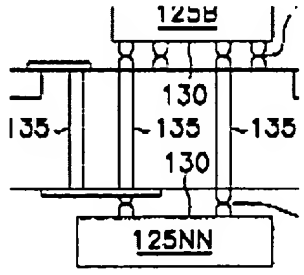


FIG. 1

5. Regarding claim 2, Ahn shows an electrically conductive material 38 disposed on the interior of the via surface of one or more carrier substrate vias to form an electrical conductive path from the top surface of the carrier substrate to the bottom surface of the carrier substrate (see fig. 3e).

6. Regarding claim 3, Ahn shows a first thin film interconnect formed on the top surface of the carrier substrate and a second thin film interconnect formed on the bottom surface of the carrier substrate, the first and second thin film interconnect defining a first pad layer and a second pad layer and further comprising one or more conductive paths 135 from the first and second pad layers to the electrically conductive.



7. Regarding claim 11, Ahn shows that the first pad and the second pad define a first and second metallurgy (col. 3/lls. 60-67 & col. 4/lls. 1-25).

8. Regarding claim 13, Ahn teaches that the carrier substrate vias are in proximate disposition the carrier substrate cavity.

9. Regarding claim 15, Ahn teaches that the carrier substrate is silicon (col. 3/lls. 63).

10. Regarding claim 16, Ahn teaches one or more circuitry manufacture comprises a conductive material 38/40 (col. 8/lls. 10-18).

11. Regarding claim 25, Ahn teaches (e.g. fig. 1) an integrated circuit apparatus 110 for facilitating the interconnection of one or more circuitry manufacture, comprising: means for defining a top carrier substrate surface and a bottom carrier substrate surface and for receiving one or more circuitry manufacture on the top carrier substrate surface and the bottom carrier substrate surface (e.g. bumps 131, traces); means for defining vias (e.g. 18) from the top carrier substrate surface to the bottom carrier substrate surface and for defining interior via surfaces for receiving one or more circuitry manufacture (conductive layer 38); and means for defining cavity surfaces on the top and/or bottom carrier substrate surfaces and for receiving one or more circuitry manufacture on the interior cavity surfaces (e.g. 141, 145, 171).

12. Regarding claim 26, Ahn teaches means (e.g. 40) for creating an electrically conductive connection through the means for defining vias on the interior via surfaces.

13. Regarding claim 27, Ahn (e.g. fig. 1) teaches an integrated circuit, comprising: a carrier substrate 110 defining a top surface and a bottom surface, the carrier substrate configured to receive one or more circuitry manufacture (i.e. traces or bumps 131) on the top surface and the bottom surface; one or more carrier substrate vias 18

penetrating the carrier substrate so that the carrier substrate vias define vias from the top surface to the bottom surface of the carrier substrate and further define interior via surfaces (see fig. 3b), the one or more carrier substrate vias configured to receive one or more circuitry manufacture (conductive layers 38/40) on the interior via surfaces; one or more carrier substrate cavities, the one or more carrier substrate cavities formed on the top and/or bottom surfaces of the carrier substrate, the one or more carrier substrate cavities defining interior cavity surfaces and configured to receive one or more circuitry manufacture (140, 145, 171) on the interior cavity surfaces; a first circuit device 125b mounted to the carrier substrate and further mounted relative to a carrier substrate cavity (e.g. adjacent) by one or more circuitry manufacture; and a second circuit device 125N mounted to the carrier substrate by one or more circuitry manufacture (bump, traces) and in electrical communication with the first circuit device.

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Wenzel et al. (US 6,150,724).

16. Regarding claim 4, Ahn shows most aspects of the instant invention including a first circuitry mounted 125 mounted to the carrier by one or more circuitry manufacture but does not show that the first circuitry is mounted atop a carrier substrate cavity.

Nevertheless, Wenzel (e.g. fig. 7) a first circuitry 102 mounted on a carrier substrate 106 by one or more circuitry manufacture (e.g. pad) and atop a carrier substrate cavity. According to Wenzel, this type of embodiment reduces the interconnect lengths of metal and thus the adverse effects of routing parasitics (col. 4/lls. 39-52; col. 18/lls. 49-58).

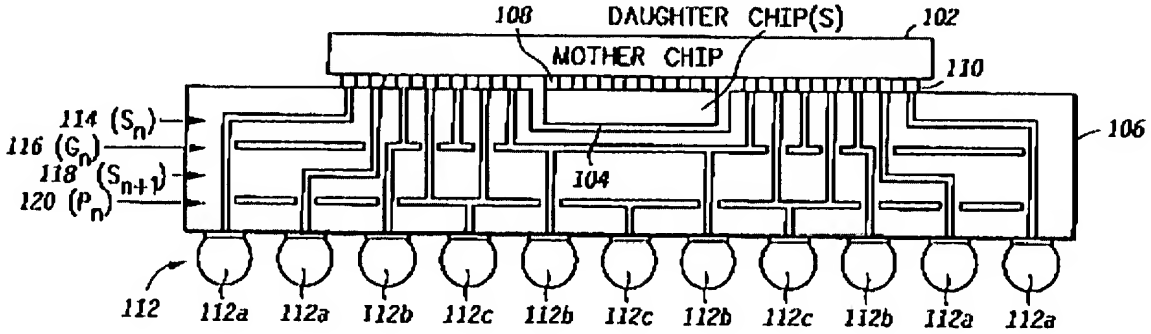


FIG. 7

It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first circuitry disclosed by Ahn over the cavity as suggested by Wenzel in order to reduce routing parasatics since the interconnection length and to minimize the IC foot print area.

17. Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Wenzel et al. (US 6,150,724) further in view of Applicant Admitted Prior Art.

18. Regarding claim 5, Ahn that the first circuitry 125 but does not explicitly teach that it comprises a MEMs. However, APA teaches that IC and MEMs devices can be packaged together (pg. 1/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first circuit device disclosed by Ahn in view of Wenzel comprising a MEMS device as suggested by APA in order to

provide a package having the capability of been remotely accessed (e.g. wireless communication, RF device, etc).

19. Regarding claim 6, Ahn further in view of Wenzel further in view of APA shows a second circuitry (125A or125AA) mounted to the carrier substrate by one or more circuitry of manufacture and proximate to one or more substrate vias.

20. Regarding claim 7, Ahn further in view of Wenzel further in view of APA shows a second circuitry (125A or 125AA) operable to communicate data (e.g. memory, processor) to and from the MEMs (125 A or 125 AA) device; and wherein the integrated circuit is in electrical communication with the MEMS device though one or more conductive paths deposited on the interior surfaces of the substrate vias.

21. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Baker et al. (US 5,869,896).

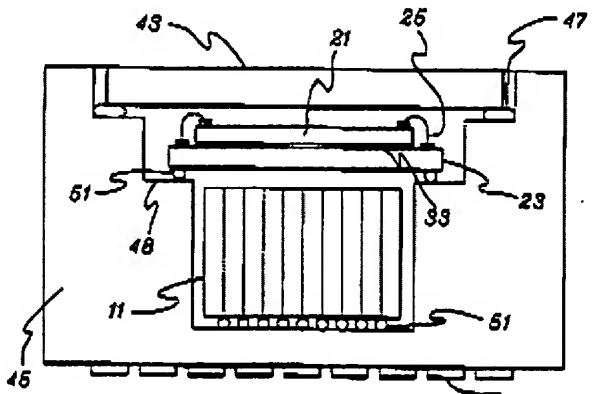


fig. 8

22. Regarding claim 8, Ahn shows most aspects of the instant invention including a first circuitry mounted to the carry substrate by one or more circuitry manufacture (bump, pads) but does not show that the first circuitry is within a carrier substrate cavity.

Nevertheless, Baker shows (e.g. fig. 8) shows a first circuitry 11 mounted on a carrier substrate cavity by one or more one or more circuitry manufacture (i.e. bumps, 51, pads, traces) and within a carrier substrate cavity (col. 6/lls. 49-58). According to Baker this type of embodiment, the individual components can be more easily reworked or replaced thereby facilitating repairs and upgrades. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first circuitry disclosed by Ahn within a carrier substrate cavity in order to provide a package that can be more easily reworked or replaced thereby facilitating repairs and upgrades as taught by Baker.

23. Regarding claim 9, Baker shows a second circuitry 23 mounted to the carrier substrate by one or more circuitry of manufacture (i.e. 51, pad, trace) and atop the carrier substrate cavity.

24. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Baker et al. (US 5,869,896) in view of Applicant Admitted Prior Art.

25. Regarding claim 10, Ahn in view of Baker teaches that the first circuitry 125 comprise a passive circuit device such as capacitors (col. 4/lls. 29-32) in n electrical communication with a second device 125 but does not explicitly teach that the second circuitry comprises MEMs. However, APA teaches that IC and MEMs devices can be packaged together (pg. 1/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make one of the IC devices disclosed by Ahn in view of Baker comprising a MEMS as suggested by APA in order to provide a

package having the capability of being remotely accessed (e.g. wireless communication, RF device, etc).

26. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over by Ahn (US 6,392,269) in view of Harper.

27. Regarding claim 12, Ahn teaches that the second metallurgy is a ball grid array but does not disclose that the first metallurgy is a wire bonding pad metallurgy. Nevertheless, Harper teaches that the use of wire bonding interconnection process prevents the degradation of the active or passive device since no external heat is used (pp. 7.29). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a wire bonding process including a wire pad metallurgy as the first pad layer in the invention disclosed by Anh to avoid degradation of the active devices since no external heat is applied during the bonding process.

28. Claims 28, 31 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Applicant Admitted Prior Art "APA".

29. Regarding claim 28, Ahn that the first circuitry 125 but does not explicitly teach that it comprises a MEMs. However, APA teaches that IC and MEMs devices can be packaged together (pg. 1/lls. 1-18). It would have been obvious to one of ordinary skill in the art at the time the invention was made to make the first circuit device disclosed by Ahn comprising a MEMS device as suggested by APA in order to provide a package having the capability of being remotely accessed (e.g. wireless communication, RF device, etc).

30. Regarding claim 31, Ahn in view of APA shows that the second device (125A or AA) is in electrical communication with the MEMS device (125A or AA) through one or more carrier substrate vias and circuitry manufacture deposited in the carrier substrate vias.

31. Regarding claim 32, Ahn in view of APA shows that the one or more circuitry of manufacture (bump, pads, traces) mounting the first and second circuitry devices to the carrier substrate comprises a thin film interconnect (e.g. trace).

32. Claims 29-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ahn (US 6,392,269) in view of Applicant Admitted Prior Art "APA" further in view of in view of Baker et al. (US 5,869,896).

33. Regarding claim 29, Ahn in view of APA shows most aspects of the instant invention including a MEMs device mounted relative to the carrier substrate cavity by one or more circuitry manufacture (bumps, pad) but does not shows tha the MEMS is in the carrier substrate cavity. Nevertheless, Baker shows (e.g. fig. 8) shows a first circuitry 11 mounted on a carrier substrate cavity by one or more one or more circuitry manufacture (i.e. bumps, 51, pads, traces) and within a carrier substrate cavity (col. 6/lls. 49-58). According to Baker this type of embodiment, the individual components can be more easily reworked or replaced thereby facilitating repairs and upgrades. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first circuitry/MEMS disclosed by Ahn in view of APA within a carrier substrate cavity in order to provide a package that can be more easily reworked or replaced thereby facilitating repairs and upgrades as taught by Baker.

34. Regarding claim 30, Ahn in view of APA shows most aspects of the instant invention including a MEMs device mounted relative to the carrier substrate cavity by one or more circuitry manufacture (bumps, pad) but does not shows that the MEMS is atop the carrier substrate cavity. Nevertheless, Baker shows (e.g. fig. 8) shows a first circuitry 23 mounted atop a carrier substrate cavity by one or more one or more circuitry manufacture (i.e. bumps, 51, pads, traces; col. 6/lls. 49-58). According to Baker this type of embodiment, the individual components can be more easily reworked or replaced thereby facilitating repairs and upgrades. It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the first circuitry/MEMS disclosed by Ahn in view of APA atop a carrier substrate cavity in order to provide a package that can be more easily reworked or replaced thereby facilitating repairs and upgrades as taught by Baker.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

36. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J. Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

37. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Leonardo Andújar
Primary Examiner
Art Unit 2826